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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,101	07/08/2003	Michael A. Filippo	5500-89400	8643

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EXAMINER	
CODY, DILLON J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,101	FILIPPO ET AL.	
	Examiner	Art Unit	
	Dillon Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *mult.*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, and declaration, all filed 8 July 2003; information disclosure statements filed 17 Nov. 2003, 18 Nov. 2003, 19 Nov 2003 and 12 May 2004; and formal drawings received 23 August 2004.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Specification

4. The disclosure is objected to because of the following informalities:

Page 2, line 7: "and" should be removed

Appropriate correction is required.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 5-6, 8-22, 24-25 and 27-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Webb et al. (U.S. Patent No. 6,360,314) hereinafter referred to as Webb.

8. As per claims 1 and 14, Webb discloses a microprocessor and computer system, comprising: a dispatch unit configured to dispatch load and store operations (Fi.g 1 clock cycle: Issue) *The examiner asserts that a unit is responsible for issuing operations*; and a load store unit configured to store information associated with load and store operations dispatched by the dispatch unit (Fig. 4), wherein the load store unit includes a STLF (Store-to-Load Forwarding) buffer (Fig. 4 buffer 428 and queue 426), wherein STLF buffer includes a plurality of entries (Fig. 7); wherein the load store unit is configured to generate an index dependent on at least a portion of an address of a load operation, to use the index to select one of the plurality of entries (Col. 5 lines 5-8 and 19-22), and to forward data included in the one of the plurality of entries as a result of the load operation. (Col. 2 lines 8-15)

9. As per claims 2 and 15, Webb discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit is configured to not forward the data included in the one of the plurality of entries as the result of the load operation if information included in the one of the plurality of entries does not match information associated with the load operation. (Col. 2 lines 7-15) *The examiner asserts that if the address does not match, an entry is not forwarded on a data load operation.*

10. As per claims 3 and 22, Webb discloses the microprocessor of claim 1 and the method of claim 20, wherein the one of the plurality of entries in the STLF buffer (Fig. 7) is configured to store an address (Fig. 7 address 42), data (Fig. 7 word 52), and a data size (Fig. 7 size 48) associated with a store operation.

11. As per claims 5, 16 and 22, Webb discloses the microprocessor of claim 1, computer system of claim 14 and the method of claim 20, wherein the load store unit is configured to select which one of the plurality of entries to allocate to a store operation by generating an additional index dependent on at least a portion an address of the store operation. (Col. 5 lines 5-8 and 19-23)

12. As per claims 6, 17 and 25, Webb discloses the microprocessor of claim 5, computer system of claim 14 and the method of claim 24, wherein the load store unit is configured to generate the additional index dependent on both the at least the portion of the address of the store operation (Col. 5 lines 5-8 and 19-23) and a number of bytes of

data operated on by the store operation (Col. 6 lines 51-59), and wherein the load store unit is configured to generate the index dependent on both the at least the portion of the address of the load operation and a number of bytes of data operated on by the load operation. *The examiner asserts that the data size is used as an index to determine if a TRAP signal is to be generated due to a load requesting a larger block of data than was previously stored at that memory location.*

13. As per claims 8 and 27, Webb discloses the microprocessor of claim 5 and the method of claim 24, wherein the additional index comprises a portion of the address targeted by the store operation. (Col. 5 lines 19-22)

14. As per claims 9 and 18, Webb discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit further comprises a STLF checker configured to verify operation of the STLF buffer. *The examiner asserts that Webb's invention contains a unit which verifies operation, specified as the apparatus disclosed in col. 7, lines 5-8.*

15. As per claims 10 and 28, Webb discloses the microprocessor of claim 9 and the method of claim 20, wherein the STLF checker is configured to perform an associative address comparison to identify all issued store operations targeting a same address as the load operation and to implement a find-first algorithm to select a youngest issued store operation that is older than the load operation. (Col. 7 lines 3-36)

16. As per claims 11, 19 and 29, Webb discloses the microprocessor of claim 9, computer system of claim 14 and the method of claim 28, wherein the STLF checker is configured to replay the load operation if the STLF checker identifies incorrect operation of the STLF buffer. (Col. 1 lines 34-38) *The examiner asserts that if a load operation does not result in data being provided from the cache, the memory load is replayed to main memory.*

17. As per claims 12 and 30, Webb discloses the microprocessor of claim 9 and the method of claim 28, wherein the STLF checker is configured to replay one or more additional operations that are dependent on the load operation if the STLF checker detects incorrect operation of the STLF buffer. (Col. 7 lines 63-65) *The examiner asserts that after the inflight instructions are killed, they must inherently be reissued. If the instructions are not reissued, the program may produce undesired output or simply cease operation.*

18. As per claims 13 and 31, Webb discloses the microprocessor of claim 9 and the method of claim 28, wherein the load store unit is configured to identify the result of the load operation as a speculative value in response to forwarding the data in the one of the plurality of entries included in the STLF buffer as the result of the load operation; wherein if the STLF checker verifies that the STLF buffer operated correctly for the load operation, the load store unit is configured to indicate that the result of the load

operation is not speculative. *The examiner asserts that while a load operation is pending in the store buffer/queue (while the address lookup is operating) the operation is speculative, as no data has yet been forwarded. When the index has been calculated, and the apparatus determines the entry to be the youngest and of the correct size, the data is forwarded and is then no longer considered speculative.*

19. As per claim 20, Webb discloses a method, comprising: receiving an address of a load operation; generating an index corresponding to the address; using the index to select an entry from a plurality of entries included in a STLF (Store-to-Load Forwarding) buffer; and forwarding data included the entry as a result of the load operation. (Col. 5 lines 5-22)

20. As per claim 21, Webb discloses the method of claim 20, wherein said forwarding is dependent on information included in the entry matching information associated with the load operation. *The examiner asserts that the forwarding of an entry is dependant on the physical address matching.*

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 4 and 23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb.

23. As per claims 4 and 23, Webb discloses the microprocessor of claim 1 and the method of claim 20, but fails to disclose each of the plurality of entries in the STLF buffer has a capacity to store a maximum amount of data that can be written by a store operation. Webb further discloses the data entry to hold any of a quadword, longword, word or byte (Col. 4 line 66-67) but does not disclose the data bus width of the processor of his invention.

24. Data buses of sizes 8, 16, 32 or 64-bit are extremely well known in the art. With any of these data buses in place in Webb's invention, the data buffer would be able to hold at least the maximum amount of data specified by a data store operation.

25. A data bus having a given size less than or equal to 64 bits is beneficial in a processor in that costs of implementation are limited. Larger data buses require processor components to also grow in size, increasing processor area, power consumption and cost.

26. Implementing a data bus less than or equal to 64 bits in Webb's invention would have been obvious at the time of invention to one of ordinary skill in the art for the benefit of limiting costs, size and power consumption.

Claims 7 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb in view of Hennessy (Hennessy, J. L., Patterson, D. A. Computer Organization and Design. Morgan Kaufmann Publishers, Inc.: 1998. Pages 549-550.)

27. As per claims 7 and 26, Webb discloses the microprocessor of claim 6 and the method of claim 25, but fails to disclose that the additional index is generated by right-shifting a lower portion of the address targeted by the store operation by an amount equal to a logarithm in base two of the number of bytes of data operated on by the store operation.

28. Hennessy discloses indexing a cache by means of the lower portion of an address, minus the appropriate offset for minimum memory access size (byte, in Hennessy's case) (Fig. 7.7 and page 549-550) Right shifting is an extremely well-known method of eliminating undesired bits to the right of desired bits.

29. Hennessy teaches that removing the two bits for the byte offset reduces the total cache size, as fewer bits must be kept in the tag field of each entry. A smaller cache size takes up less space on chip and is less expensive to implement.

30. It would have been obvious to one of ordinary skill in the art at the time of invention to have included the method of generating a cache index disclosed by Hennessy in Webb's invention for the benefit of reducing necessary cache size.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Huges et al. (U.S. Patent No. 6,549,990) disclose a system implementing forwarding of store/load operations.

32. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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